

DATA SHEET



TSA5055T

2.65 GHz bidirectional I²C-bus
controlled synthesizer

Product specification
Supersedes data of November 1991
File under Integrated Circuits, IC02

1999 Aug 11

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

FEATURES

- Complete 2.65 GHz single-chip system
- Low power 5 V, 60 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- 5-level Analog to Digital Converter (ADC)
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 6 controllable outputs, 4 bidirectional
- Power-down flag
- Available in SOT109-1 (SO16) package
- Symmetrical or asymmetrical drive.

APPLICATIONS

- Satellite TV
- High IF cable tuning systems.



GENERAL DESCRIPTION

The TSA5055T is a single-chip PLL frequency synthesizer designed for satellite TV tuning systems. It may be used with a symmetrical input (pins 13 and 14) or with an asymmetrical input (pin 13).

Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the six output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning these ports can be read out of the TSA5055T on the SDA line (one status byte) during a READ operation. A flag is set when the loop is 'in-lock' and is read during a READ operation. The device has one fixed I²C-bus address and three programmable addresses, programmed by applying a specific voltage to port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	supply voltage	4.5	5	5.5	V
I _{CC}	supply current	–	60	80	mA
f _{RF}	RF input frequency range	1	–	2.65	GHz
V _{I (rms)}	input voltage level (RMS value)				
	1 to 1.8 GHz	50	–	300	mV
	1.8 to 2.65 GHz	70	–	300	mV
f _{XTAL}	crystal oscillator frequency	3.2	4	4.48	MHz
Z _{XTAL}	crystal oscillator impedance (absolute value)	600	1000	–	Ω
I _o	open-collector output current P7, P6, P5 and P4	–	–	10	mA
	output current P3 and P0	–	1	–	mA
T _{amb}	ambient temperature	–20	–	+85	°C
T _{stg}	storage temperature	–40	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	CODE
TSA5055T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

BLOCK DIAGRAM

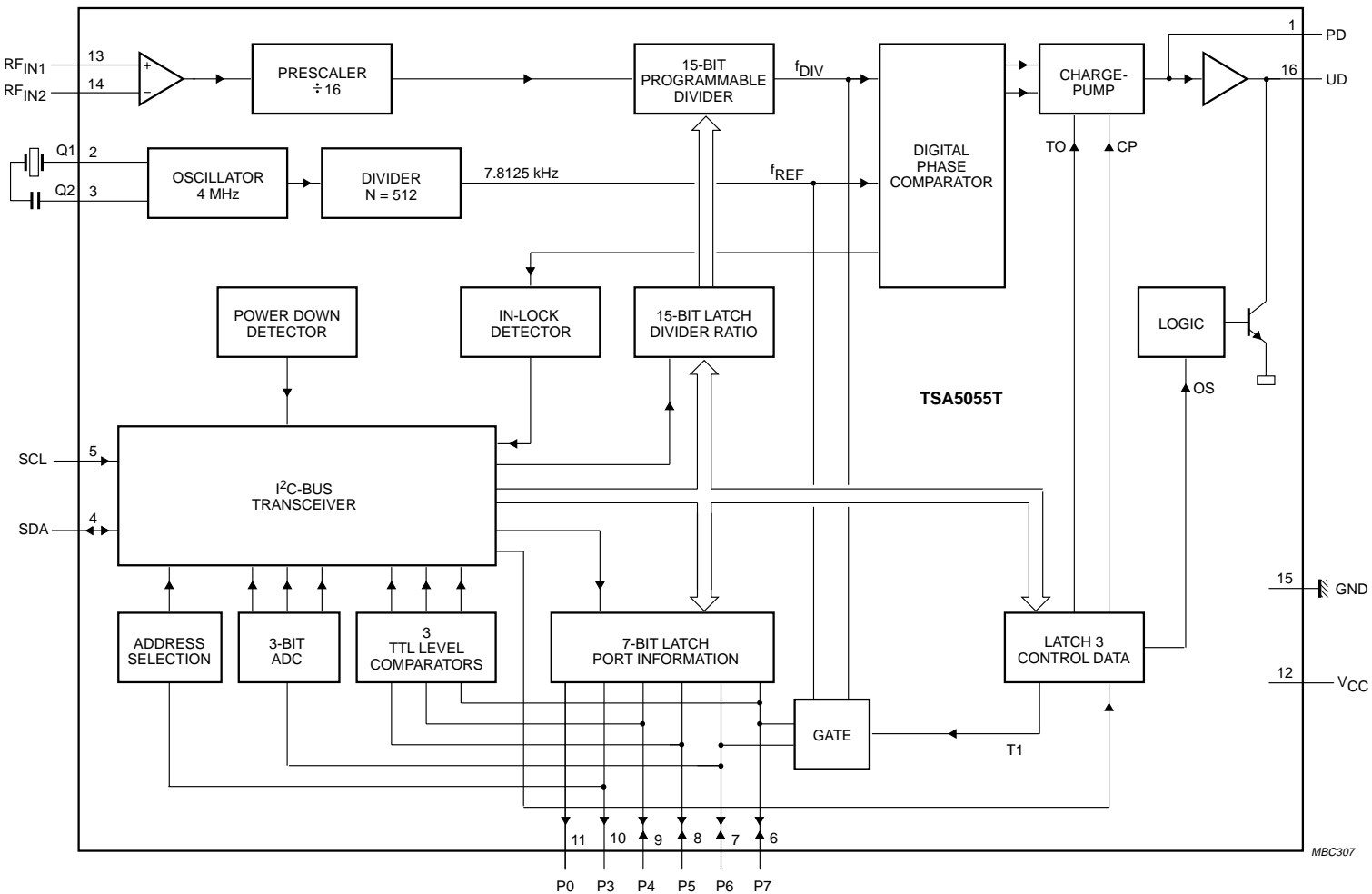


Fig.1 Block diagram.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output/input (general purpose)
P6	7	port output/input (ADC)
P5	8	port output/input (general purpose)
P4	9	port output/input (general purpose)
P3	10	port output (also used for address selection)
P0	11	port output
V _{CC}	12	voltage supply
RF _{IN1}	13	RF signal input 1
RF _{IN2}	14	RF signal input 2 (decoupled)
GND	15	ground
UD	16	drive output

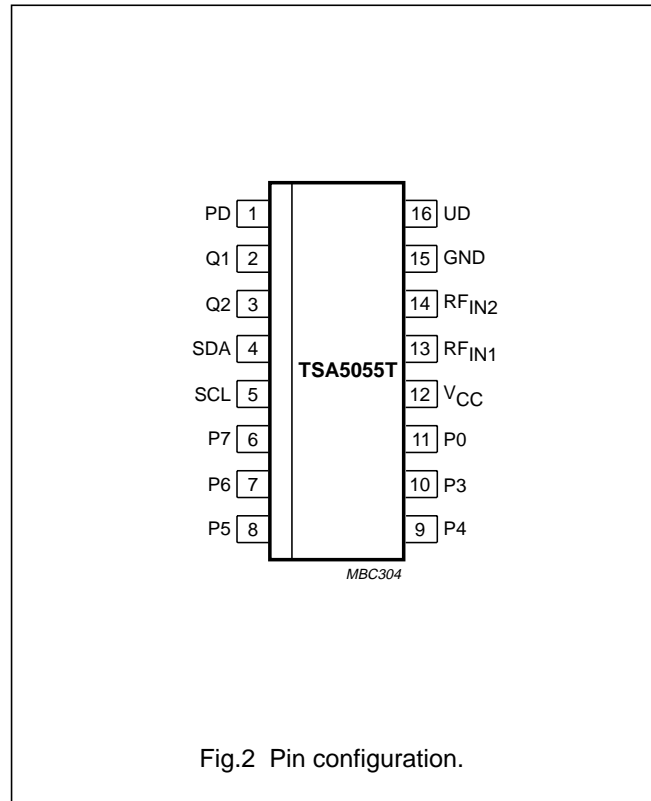


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The TSA5055T is controlled via the 2-wire I²C-bus. For programming, there is one (7-bit) module address and the R/W bit for selecting READ or WRITE mode.

WRITE mode: $R/\bar{W} = 0$; see Table 1

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5055T. The bus transceiver has an auto-increment facility that permits the programming of the TSA5055T within one single transmission (address + four data bytes).

The TSA5055T can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4.

The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge-pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high-impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the RF signal is first divided by 16, the step size is 125 kHz. A 3.2 MHz crystal can offer a step size of 100 kHz.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

Table 1 Write data format; see notes 1 to 13

BYTE	DATA BYTE								COMMAND	
	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
		N7	N6	N5	N4	N3	N2	N1	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports, control bits	P7	P6	P5	P4	P3	X	X	P0	A	byte 5

Notes

- MA1 and MA0: programmable address bits (see Table 3).
- A: Acknowledge bit.
- N14 to N0: programmable divider bits.
- $N = N14 \times 2^{14} + N13 \times 2^{13} + \dots + N1 \times 2^1 + N0$.
- CP: charge-pump current. CP = 0: 50 μ A; CP = 1: 220 μ A.
- P7 to P4 = 1: open-collector outputs are active.
- P7 to P3 and P0 = 0: outputs are in high-impedance state.
- P3 and P0 = 1: current-limited outputs are active.
- T1, T0 and OS = 0, 0 and 0: normal operation.
- T1 = 1: P6 = f_{REF} and P7 = f_{DIV} .
- T0 = 1: 3-state charge-pump.
- OS = 1: Operational amplifier output is switched off (varicap drive disable).
- X: don't care.

READ mode: $R/\overline{W} = 1$; see Table 2

Data can be read out of the TSA5055T by setting the R/\overline{W} bit to 1. After the slave address has been recognized, the TSA5055T generates an Acknowledge signal (A) and the first data byte (status byte) is transferred to the SDA line (MSB first). Data is valid on the SDA line while the SCL clock signal is HIGH.

A second data byte can be read out of the TSA5055T if the processor generates an Acknowledge signal on the SDA line. End of transmission will occur if the processor does not send an Acknowledge signal.

The TSA5055T will then release the data line to allow the processor to generate a STOP condition. When ports P3 to P7 are used as inputs, they must be programmed to their high-impedance state.

The POR flag (Power-On Reset) is set to 1 at power-on and when V_{CC} goes below 3 V. The flag is reset when an end of data is detected by the TSA5055T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates when the loop is phase-locked (FL = 1).

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

Table 2 Read data format (see notes 1 to 5)

BYTE	MSB		DATA BYTE				LSB		COMMAND	
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

Notes

1. POR: Power-on reset flag (POR = 1 on power-on).
2. FL: in-lock flag (FL = 1 when the loop is phase-locked).
3. I2, I1 and I0: digital information for I/O ports P7, P5 and P4 respectively.
4. A2, A1 and A0: digital outputs of the 5-level ADC. Accuracy is $\frac{1}{2}$ LSB (see Table 4).
5. MSB is transmitted first.

Bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4, respectively. A logic '0' indicates a LOW level and a logic '1' a HIGH level (TTL levels). A built-in 5-level ADC is available at I/O port P6. This ADC can be used to feed AFC information to the controller from the IF section of the receiver, as shown in Fig.4. The relationship between bits A2, A1, A0 and the input voltage at port P6 is given in Table 4.

Table 3 Address selection

MA1	MA0	VOLTAGE APPLIED ON PORT P3
0	0	0 to 0.1V _{CC}
0	1	always valid
1	0	0.4V _{CC} to 0.6V _{CC}
1	1	0.9V _{CC} to 13.5 V

Address selection; see Table 3

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to three) in one system. The relationship between MA1 and MA0 and the input voltage at port P3 is given in Table 3.

Table 4 ADC levels

A2	A1	A0	VOLTAGE APPLIED ON PORT P6
1	0	0	0.6V _{CC} to V _{CC}
0	1	1	0.45V _{CC} to 0.6V _{CC}
0	1	0	0.3V _{CC} to 0.45V _{CC}
0	0	1	0.15V _{CC} to 0.3V _{CC}
0	0	0	0 to 0.15V _{CC}

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

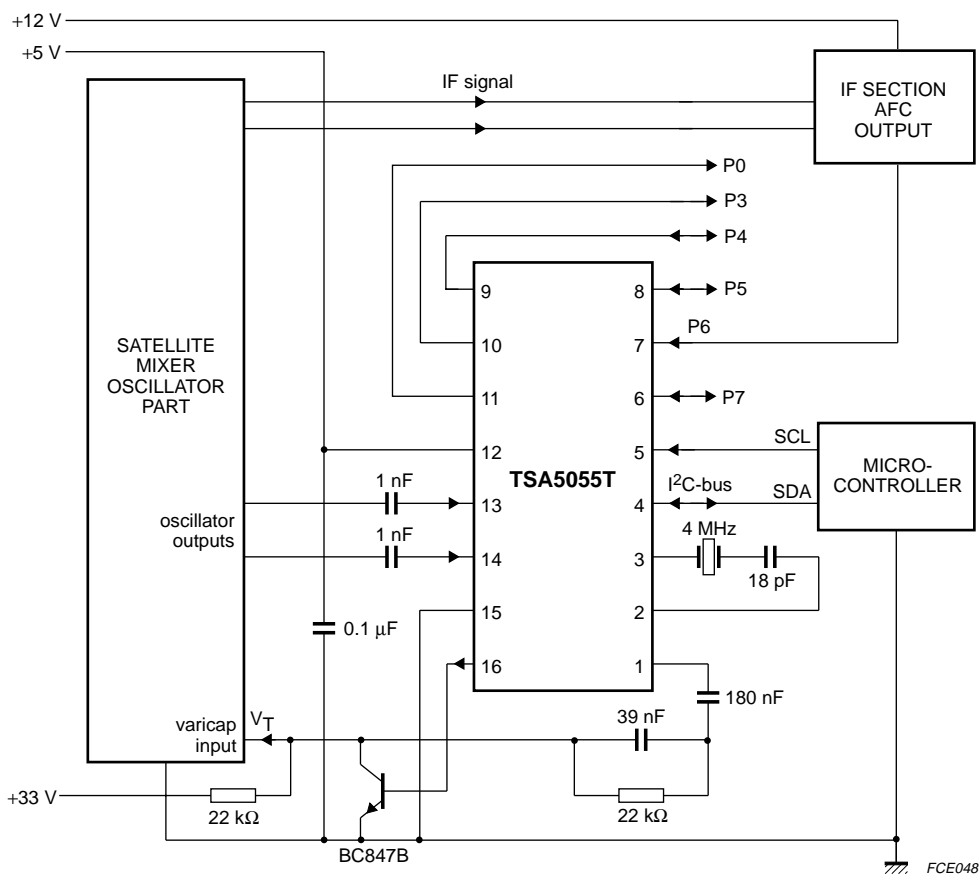


Fig.3 Symmetrical application diagram.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

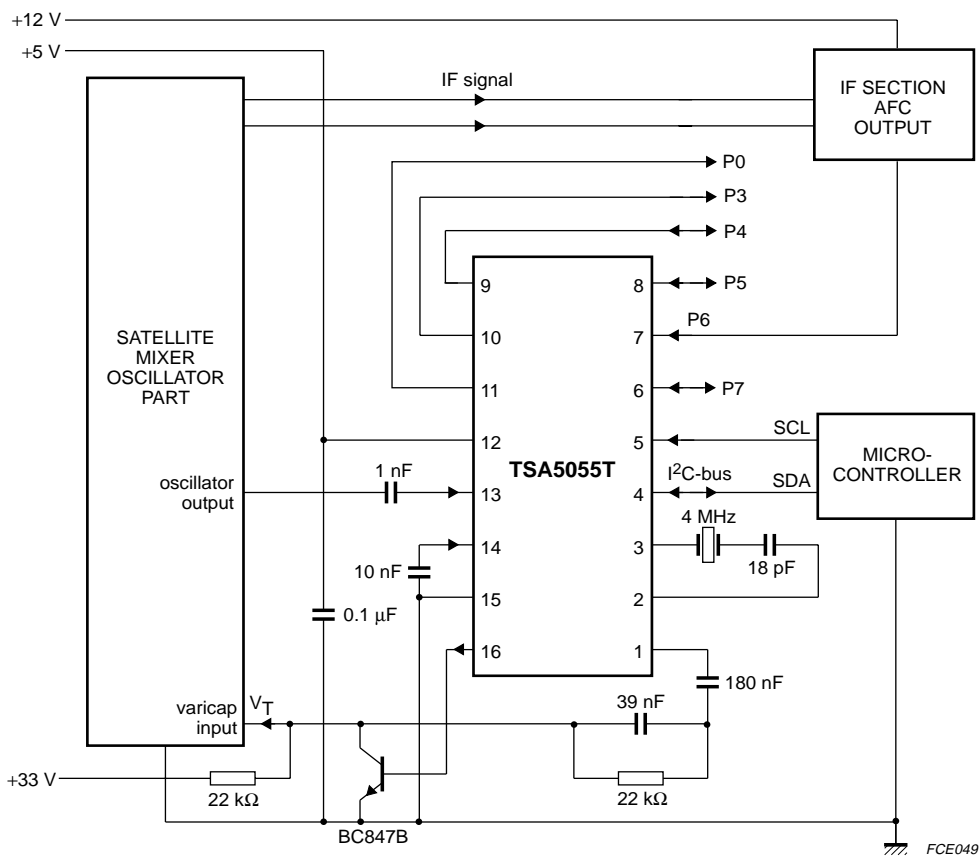


Fig.4 Asymmetrical application diagram.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{CC}	supply voltage	-0.3	+6	V
V _{O(PD)}	charge-pump (PD) output voltage	-0.3	V _{CC}	V
V _{I(Q1)}	crystal (Q1) input voltage	-0.3	V _{CC}	V
V _{I(O(SDA))}	serial data (SDA) input/output voltage	-0.3	+6	V
V _{I(SCL)}	serial clock (SCL) input voltage	-0.3	+6	V
V _{I(O(P7-P0))}	input/output ports (P7 to P3 and P0) voltage	-0.3	+16	V
V _{I(RFIN)}	prescaler inputs (RF _{IN1} and RF _{IN2}) voltage	-0.3	+2.5	V
V _{O(UD)}	drive output (UD) voltage	-0.3	V _{CC}	V
I _{O(P4-P7)}	output ports (P7 to P4) current (open-collector)	-1	+15	mA
I _{O(SDA)}	serial data (SDA) output current (open-collector)	-1	+5	mA
T _{stg}	storage temperature	-40	+150	°C
T _j	maximum junction temperature	-	150	°C

HANDLING

All pins withstand the ESD test in accordance with "MIL-STD-883C", category A (1000 V).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	from junction to ambient	in free air	110	K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{CC}	supply voltage range		4.5	5	5.5	V
T _{amb}	ambient temperature		-20	-	+85	°C
f _{RF}	RF input frequency range		1	-	2.65	GHz
N	divider ratio		256	-	32767	
I _{CC}	supply current		-	60	80	mA
f _{XTAL}	crystal oscillator frequency		3.2	4	4.48	MHz
Z _{XTAL}	crystal oscillator impedance (pin 2)	absolute value	600	1000	-	Ω
V _{XTAL(p-p)}	drive level on pin 2 (quartz Philips 4322 143 04093) (peak-to-peak value)		-	110	-	mV
V _{I(rms)}	input voltage level (RMS value) f = 1 to 1.8 GHz f = 1.8 to 2.65 GHz	V _{CC} = 4.5 to 5.5 V; T _{amb} = -20 to +85 °C; see typical sensitivity curve in Fig.5	50/-13 70/-10	- -	300/2.6 300/2.6	mV/dBm mV/dBm
R _I	prescaler input impedance	see Smith chart in Fig.6	-	50	-	Ω
C _I	input capacitance		-	2	-	pF

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

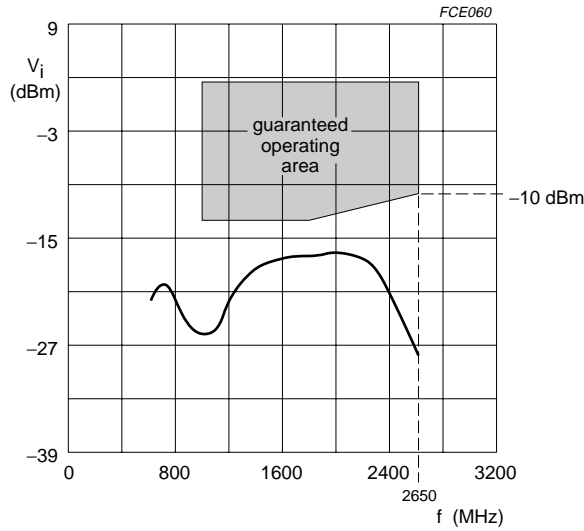
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output ports P3 and P0 (current limited)						
I _{LO}	leakage current	V _o = 13.5 V	–	–	10	μA
I _{OS}	output sink current	V _o = 13.5 V	0.7	1	1.5	mA
Output ports P7 to P4 (open collector); see note 1						
I _{LO}	leakage current	V _o = 13.5 V	–	–	10	μA
V _{OL}	output voltage LOW	I _o = 10 mA; note 2	–	–	0.7	V
Input ports P6 and P3						
I _{IH}	input current HIGH	V _{IH} = 13.5 V	–	–	10	μA
I _{IL}	input current LOW	V _{IL} = 0 V	–10	–	–	μA
Input ports P7, P5 and P4						
V _{IH}	input voltage HIGH		2.7	–	–	V
V _{IL}	input voltage LOW		–	–	0.8	V
I _{IH}	input current HIGH	V _{IH} = 13.5 V	–	–	10	μA
I _{IL}	input current LOW	V _{IL} = 0 V	–10	–	–	μA
Bus inputs SCL and SDA						
V _{IH}	input voltage HIGH		3	–	5.5	V
V _{IL}	input voltage LOW		–	–	1.5	V
I _{IH}	input current HIGH	V _{IH} = 5 V; V _{CC} = 0 V	–	–	10	μA
		V _{IH} = 5 V; V _{CC} = 5 V	–	–	10	μA
I _{IL}	input current LOW	V _{IL} = 0 V; V _{CC} = 0 V	–10	–	–	μA
		V _{IL} = 0 V; V _{CC} = 5 V	–10	–	–	μA
Output SDA (open-collector)						
I _{OH}	leakage current	V _{OH} = 5.5 V	–	–	10	μA
V _{OL}	output voltage	I _{OL} = 3 mA	–	–	0.4	V
Charge-pump output PD						
I _{OH}	output current HIGH (absolute value)	CP = 1	90	220	300	μA
I _{OL}	output current LOW (absolute value)	CP = 0	22	50	75	μA
V _O	output voltage	in-lock	1.5	–	2.5	V
I _{O(leak)}	off-state leakage current	T ₀ = 1	–5	–	+5	nA
Operational amplifier output UD (test mode: T₀ = 1)						
V _O	output voltage	V _{O(PD)} = 0 V	–	–	100	mV
	output voltage when switched off	T ₀ = 1; OS = 1; V _{O(PD)} = 2 V	–	–	250	mV
h _{FE}	operational amplifier current gain	T ₀ = 1, OS = 0; V _{O(PD)} = 2 V I _{O(UD)} = 10 μA	2000	–	–	
	$\frac{I_{O(UD)}}{I_{O(PD)} - I_{O(PD\ leak)}}$					

Notes

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector active.

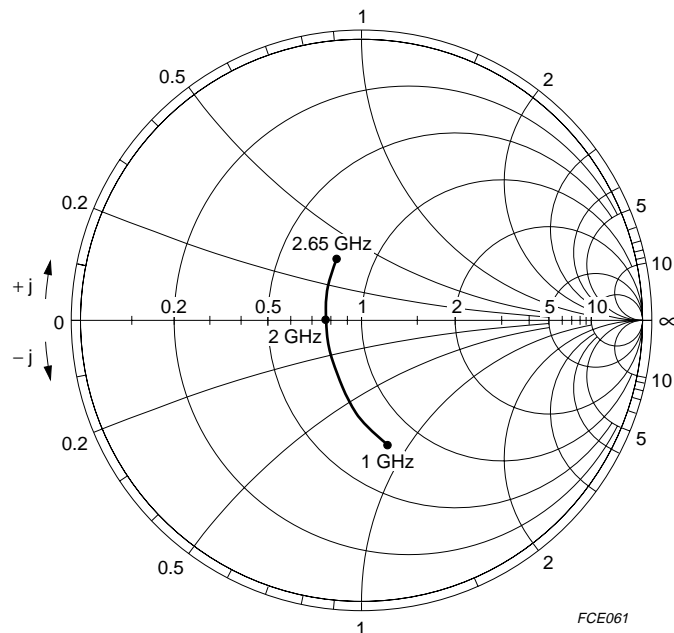
2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T



V_{CC} = 5 V; T_{amb} = 25 °C.

Fig.5 Typical input sensitivity curve.



V_{CC} = 5 V; reference value = 50 Ω.

Fig.6 Smith chart of typical input impedance.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm \left(\frac{K_{VCO}}{K_O} \times I_{CP} \times \frac{C1 + C2}{C1 \times C2} \right)$$

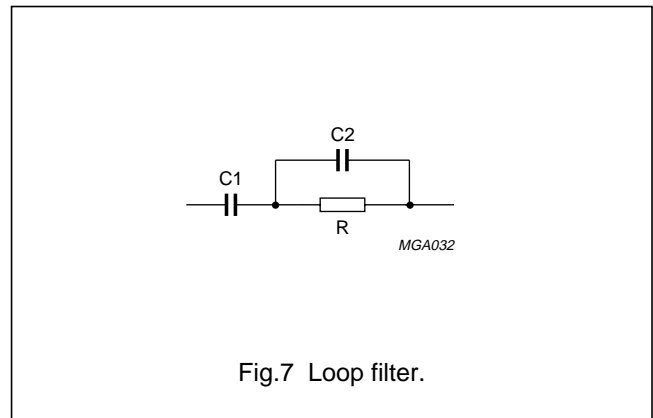
where:

K_{VCO} = oscillator slope (Hz/V)

I_{CP} = charge-pump current (A)

$K_O = 4 \times 10^6$

C1 and C2 = loop filter capacitors.



Flock flag settings

PARAMETER	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	μs
Time span between the loop losing lock and FL-flag resetting	0	128	μs

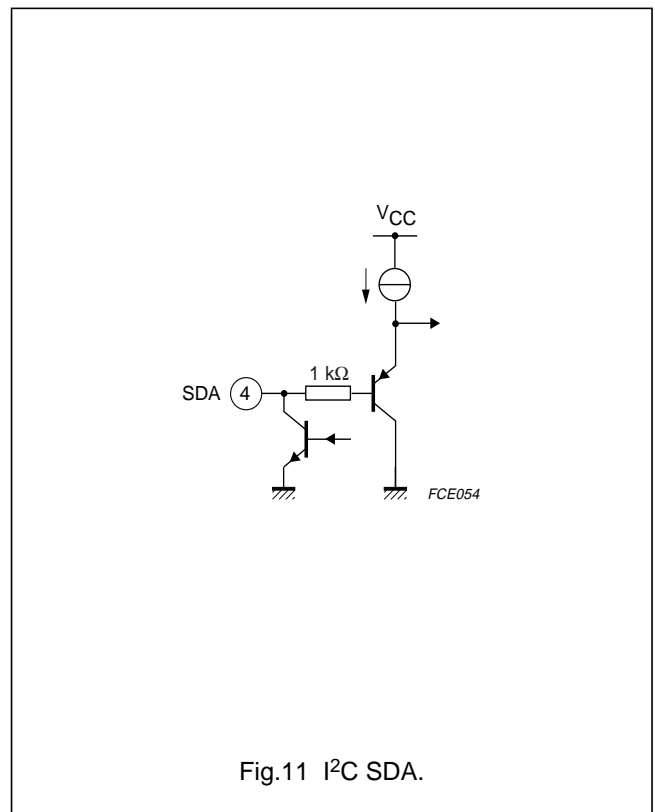
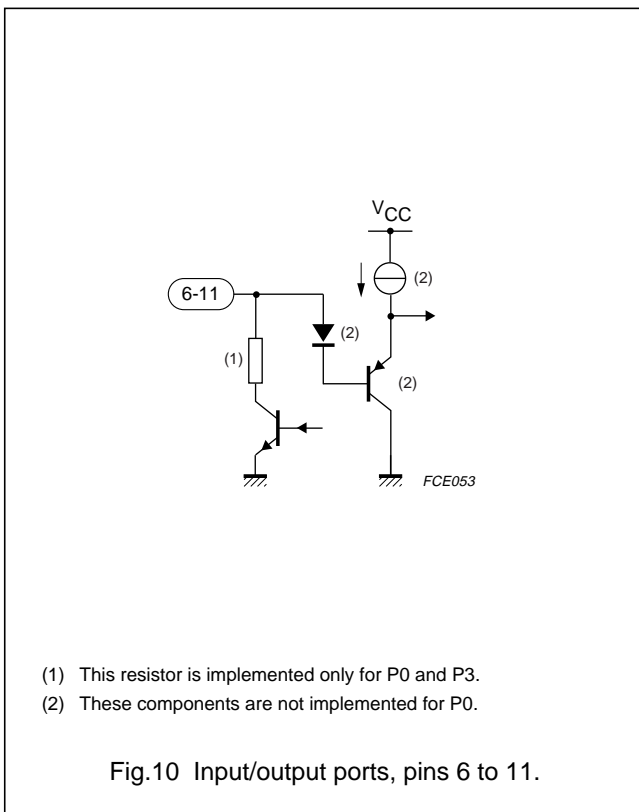
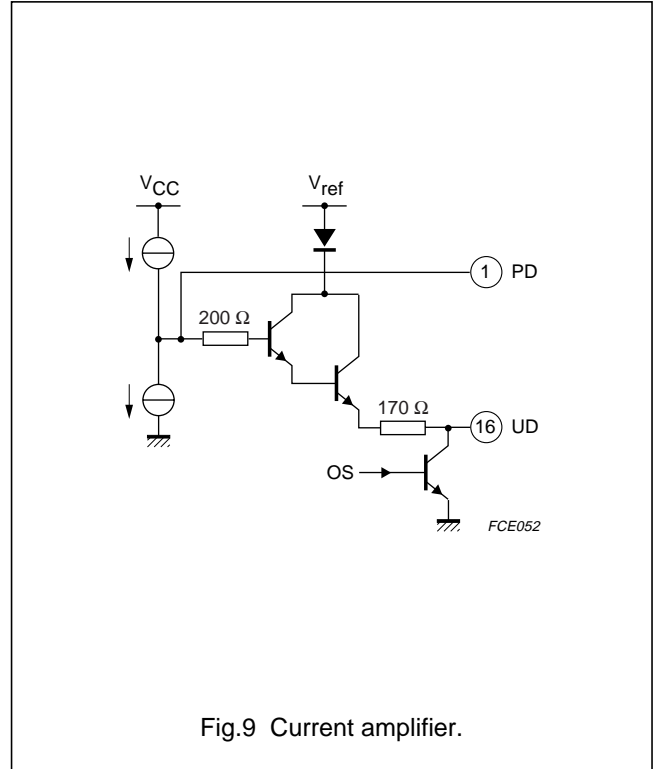
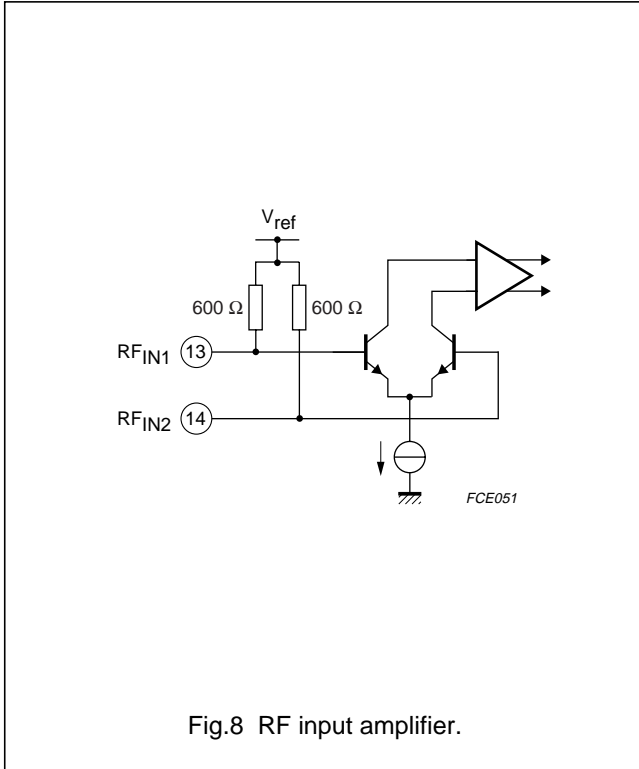
Flock flag application

- $K_{VCO} = 50 \text{ MHz/V}$
- $I_{CP} = 220 \mu A$
- $C1 = 180 \text{ nF}$
- $C2 = 39 \text{ nF}$
- $\Delta f = \pm 85.8 \text{ kHz}$.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

EQUIVALENT INPUT CIRCUITS



2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

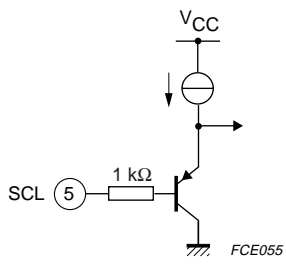


Fig.12 I²C SCL.

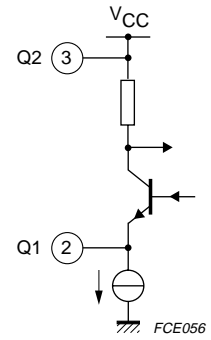


Fig.13 Reference oscillator.

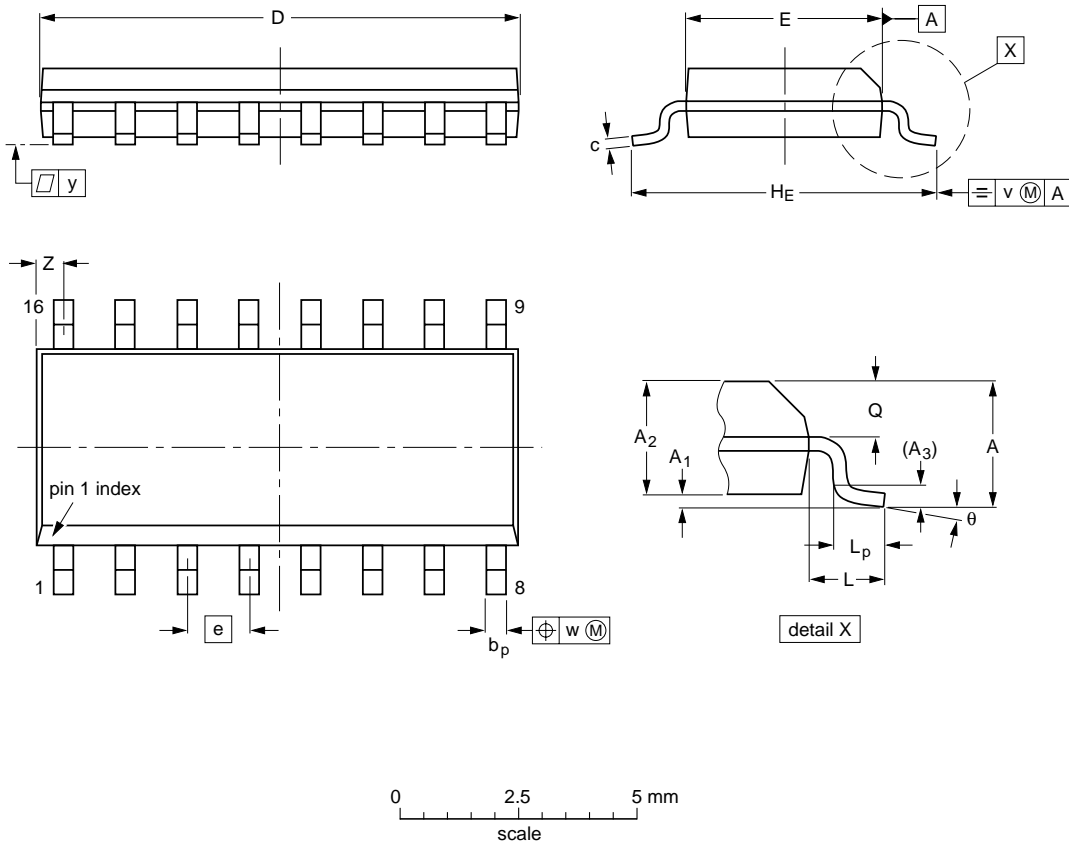
2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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2.65 GHz bidirectional I²C-bus controlled
synthesizer

TSA5055T

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